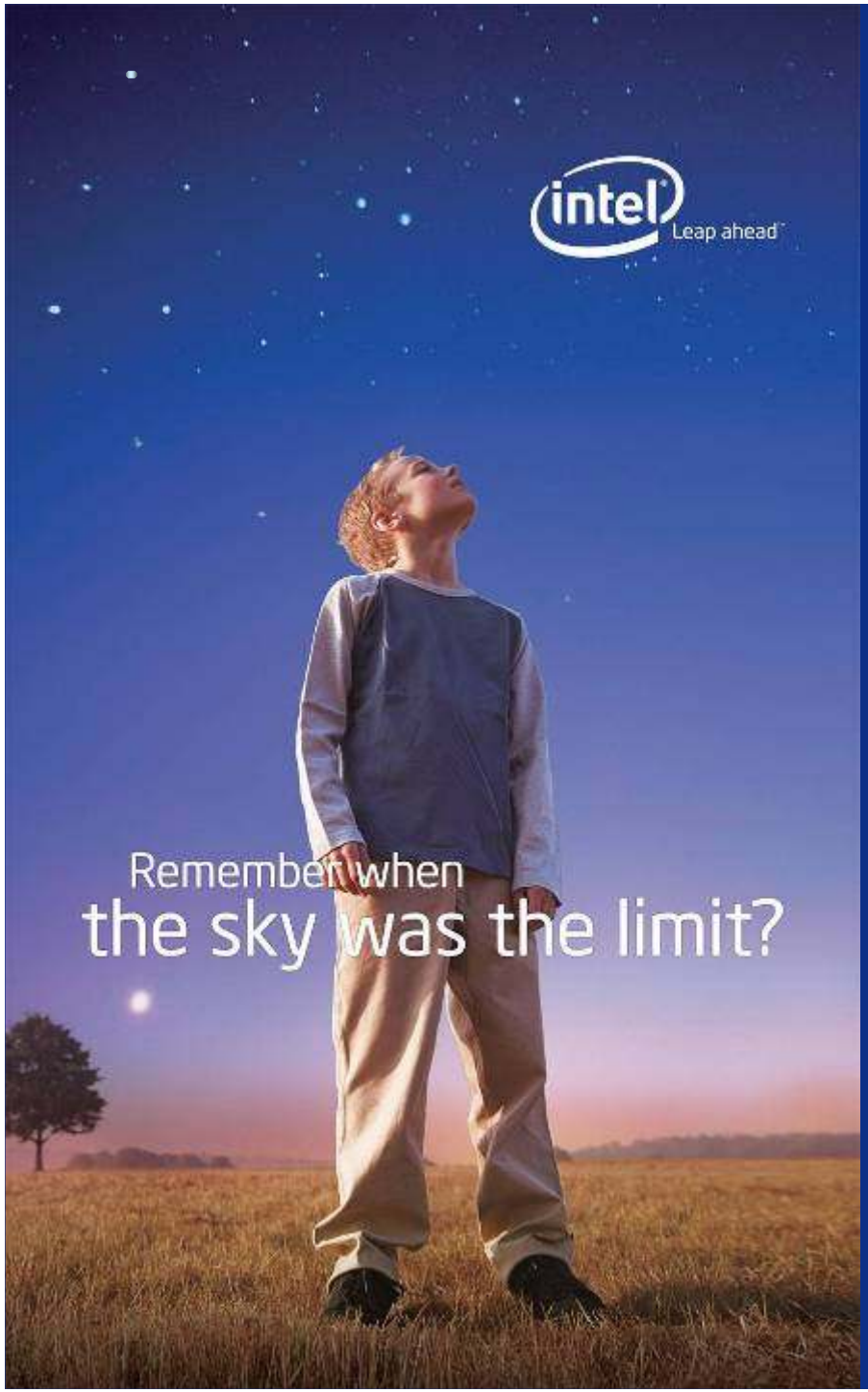
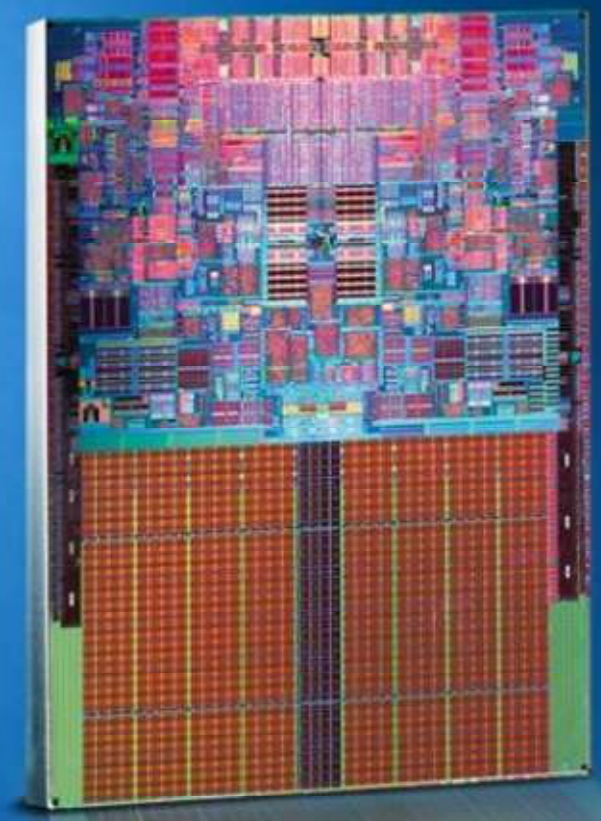


Quad-Core & Beyond Evangelism From Intel®

<Glen Skimming>
<HPC & CSM Solution Specialist>

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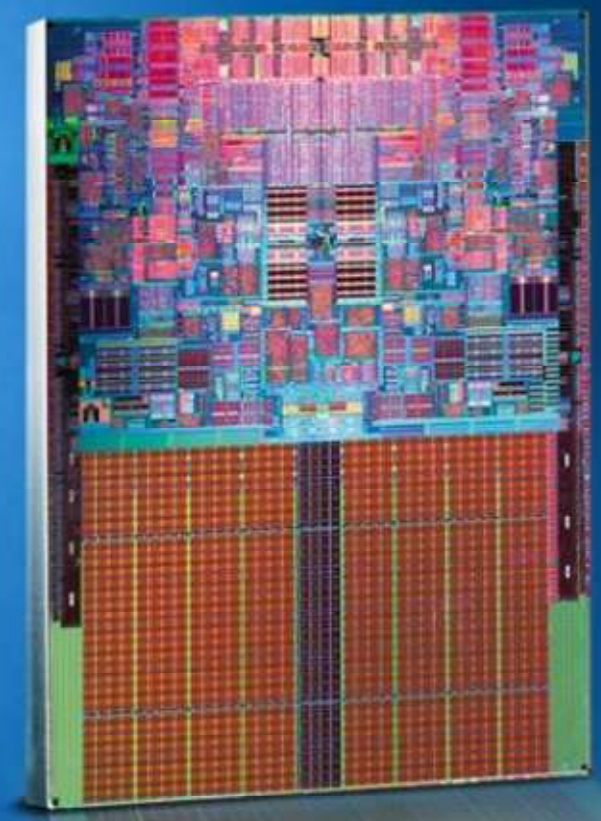
Flow



- Legal Stuff
 - Protect the presenter
- Power-point Way
 - The Intel way
- Roadmap Way
 - Affirm Intel's forward thinking
- Baseline
 - Let's agree
- Postulate
 - Now guess on what may come
- Come clean
 - We …….☺

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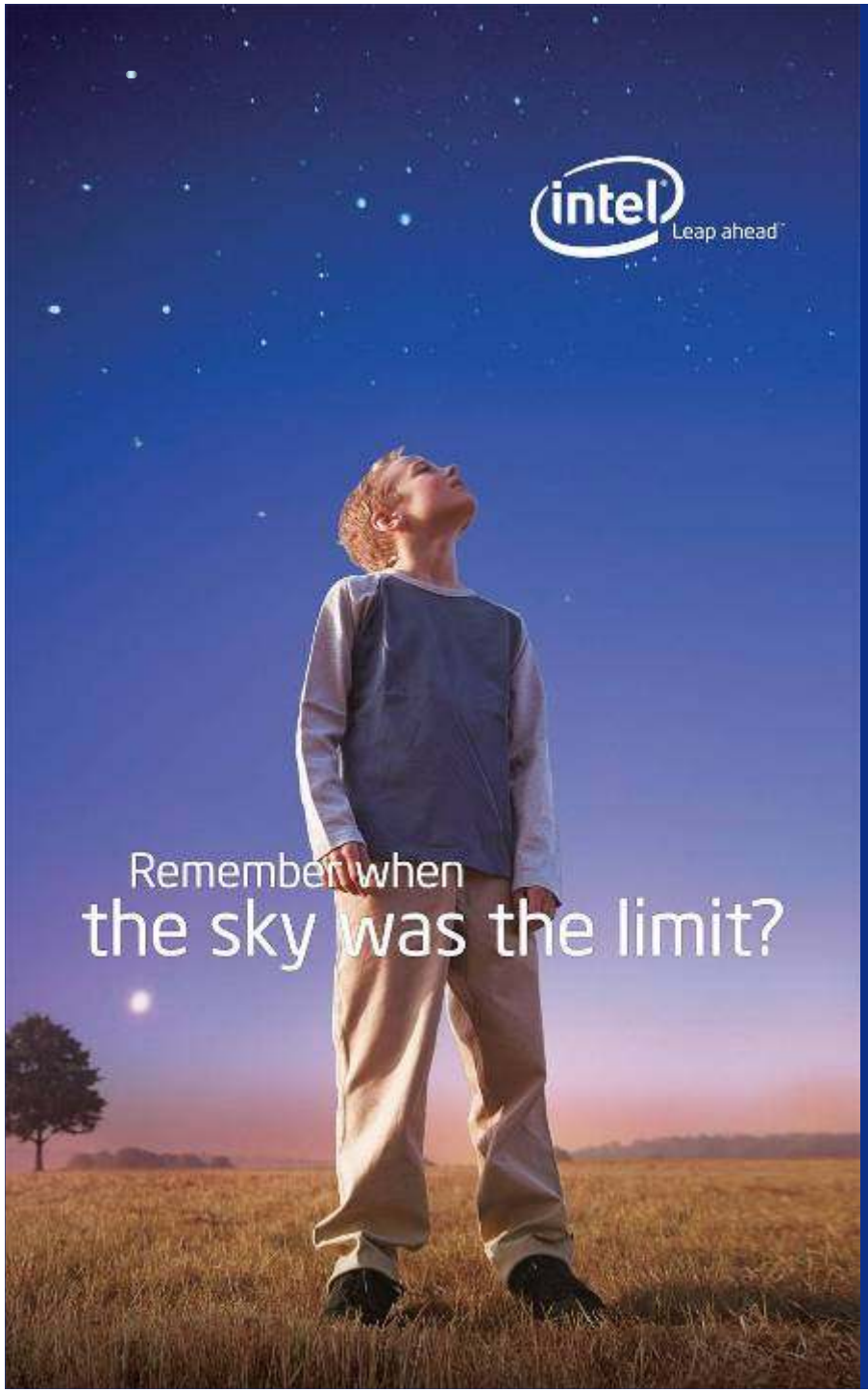
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Relative performance for each benchmark is calculated by taking the actual benchmark result for the first platform tested and assigning it a value of 1.0 as a baseline. Relative performance for the remaining platforms tested was calculated by dividing the actual benchmark result for the baseline platform into each of the specific benchmark results of each of the other platforms and assigning them a relative performance number that correlates with the performance improvements reported.

Performance per watt calculated as the benchmark result divided by the average system watts measured with an Extech* or like meter at the wall under “steady-state” load unless otherwise noted.

SPECint2000 and SPECfp2000 benchmark tests reflect the performance of the microprocessor, memory architecture and compiler of a computer system on compute-intensive, 32-bit applications. SPEC benchmark tests results for Intel microprocessors are determined using particular, well-configured systems. These results may or may not reflect the relative performance of Intel microprocessor in systems with different hardware or software designs or configurations (including compilers). Buyers should consult other sources of information, including system benchmarks; to evaluate the performance of systems they are considering purchasing.

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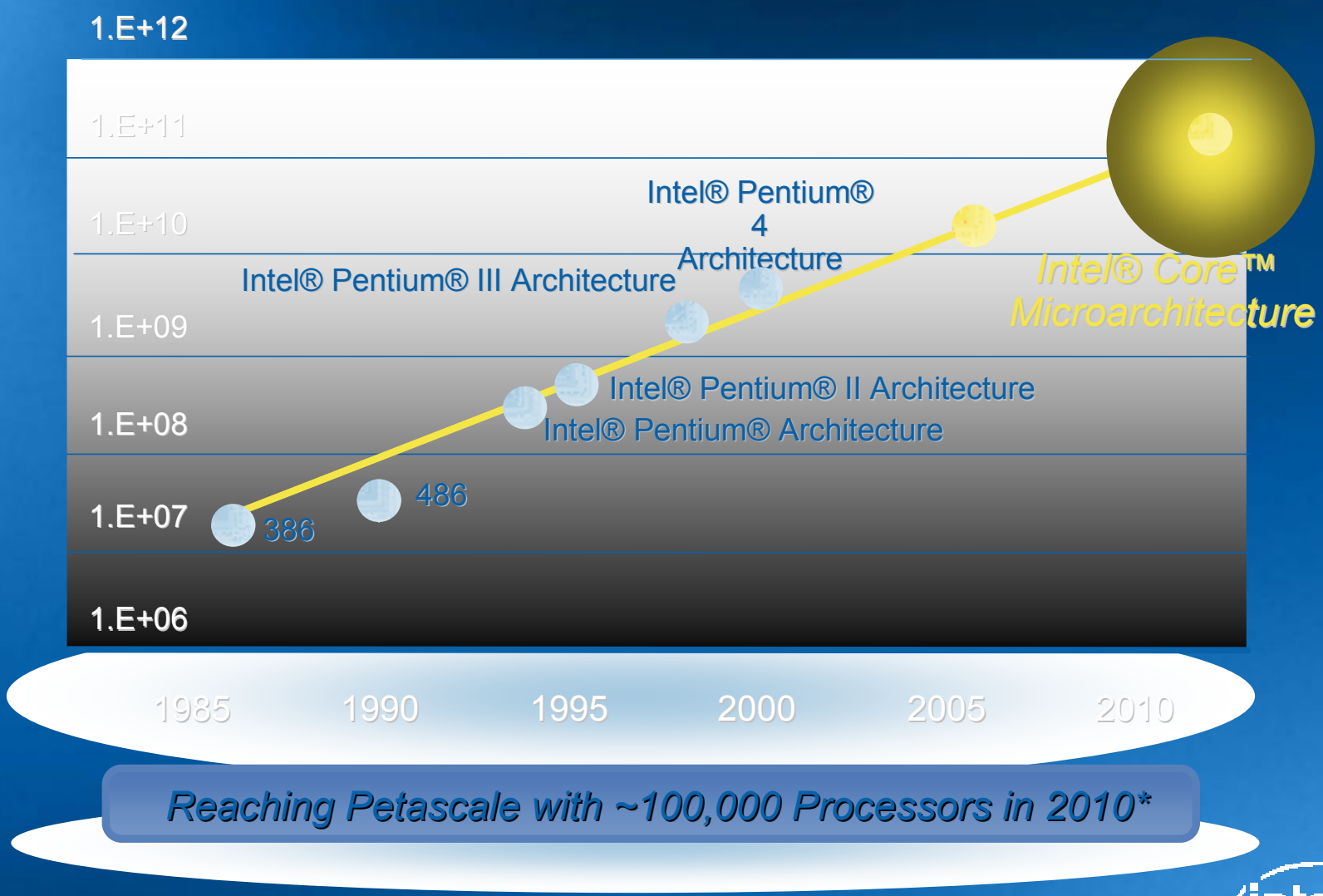
Cores the PowerPoint Way

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Processor Performance

Assuming approx. 100Glops processors
* Petascale assumes 10's of PF Peak Performance and 1PF Sustained Performance on HPC Applications.



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Beyond: Could be Multi-threaded Cores



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Beyond: Increasing Throughput through Parallelism

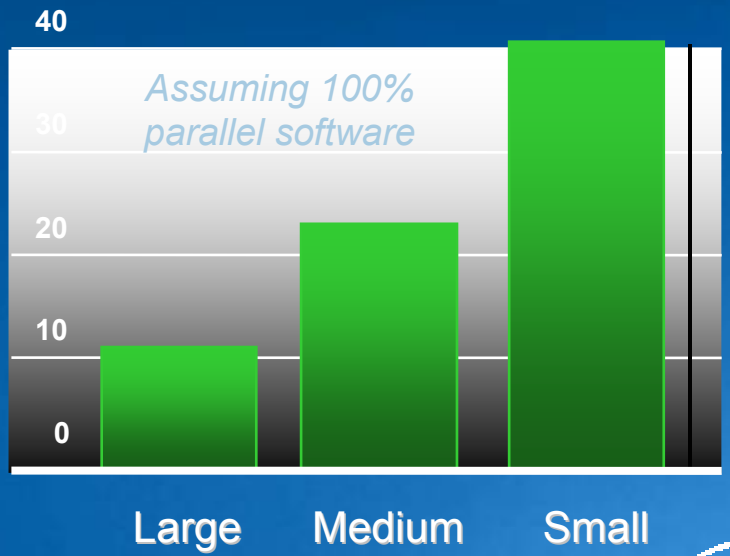
Amdahl's Law: Parallel Speedup = 1/(Serial% + (1-Serial%)/N*)



Single Core Performance
Relative Performance

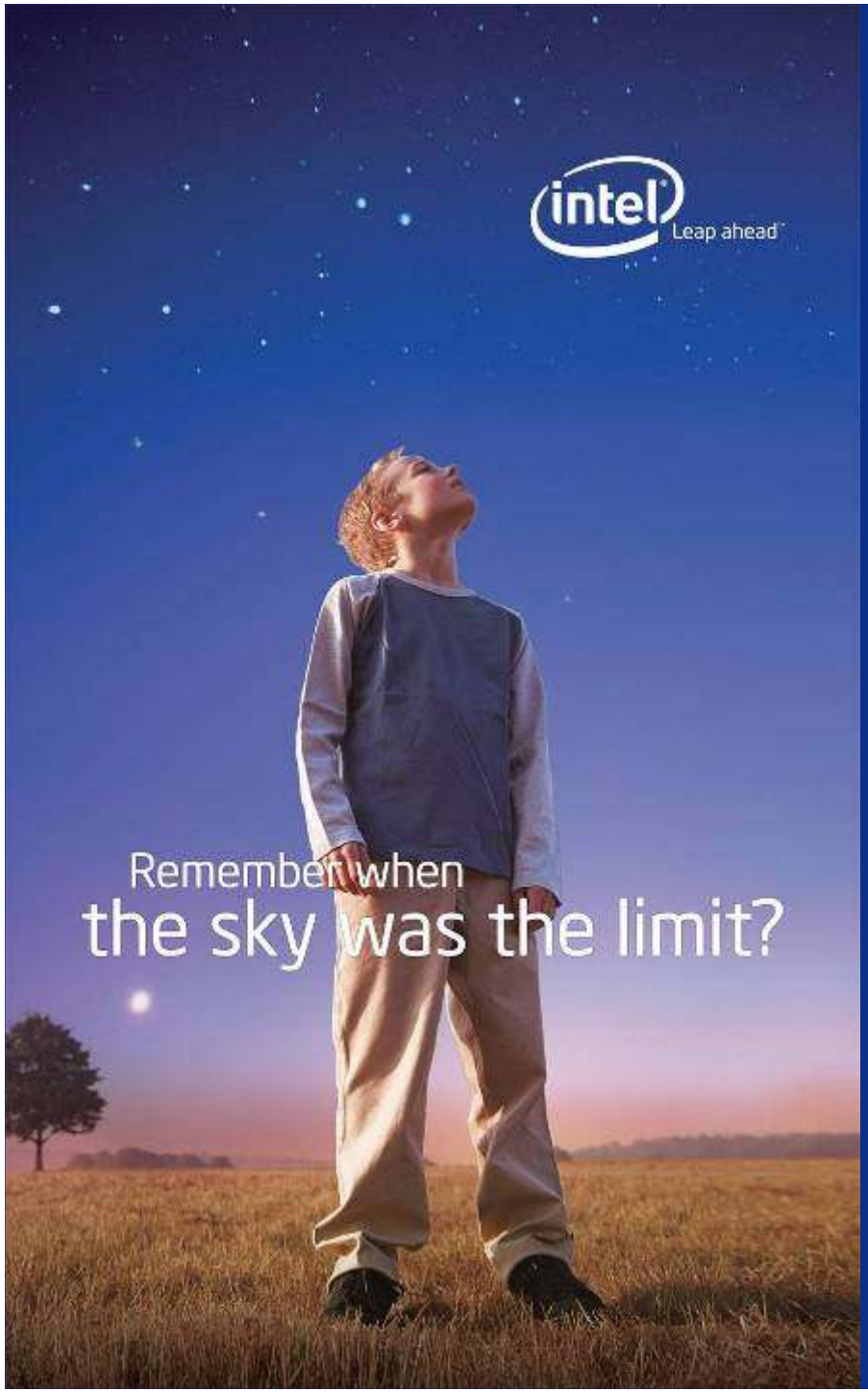


System Performance



* N = number of cores

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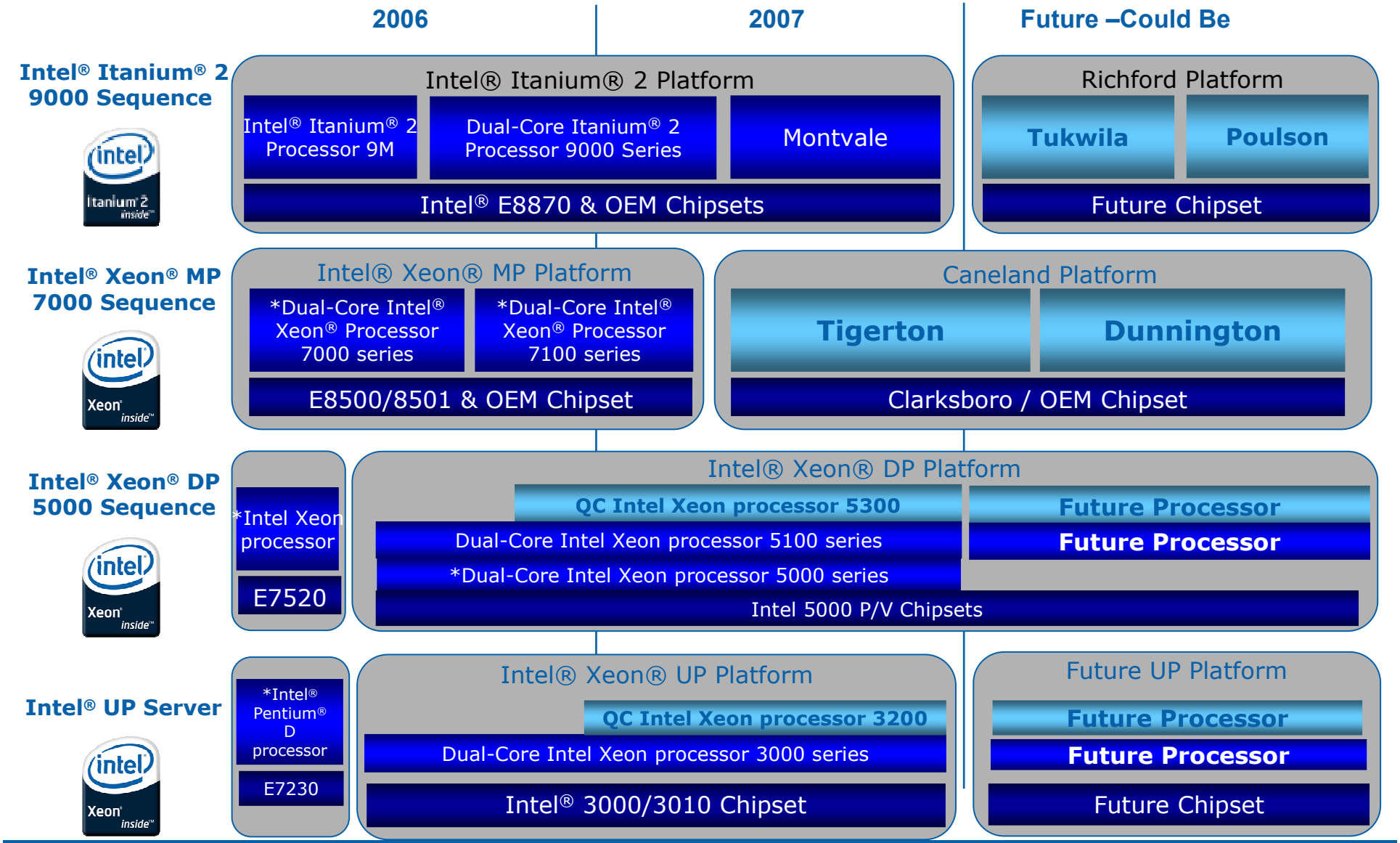


Cores the Roadmap Way

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Intel® Server Platform Roadmap



4+ Cores

Intel® Core™ Microarchitecture

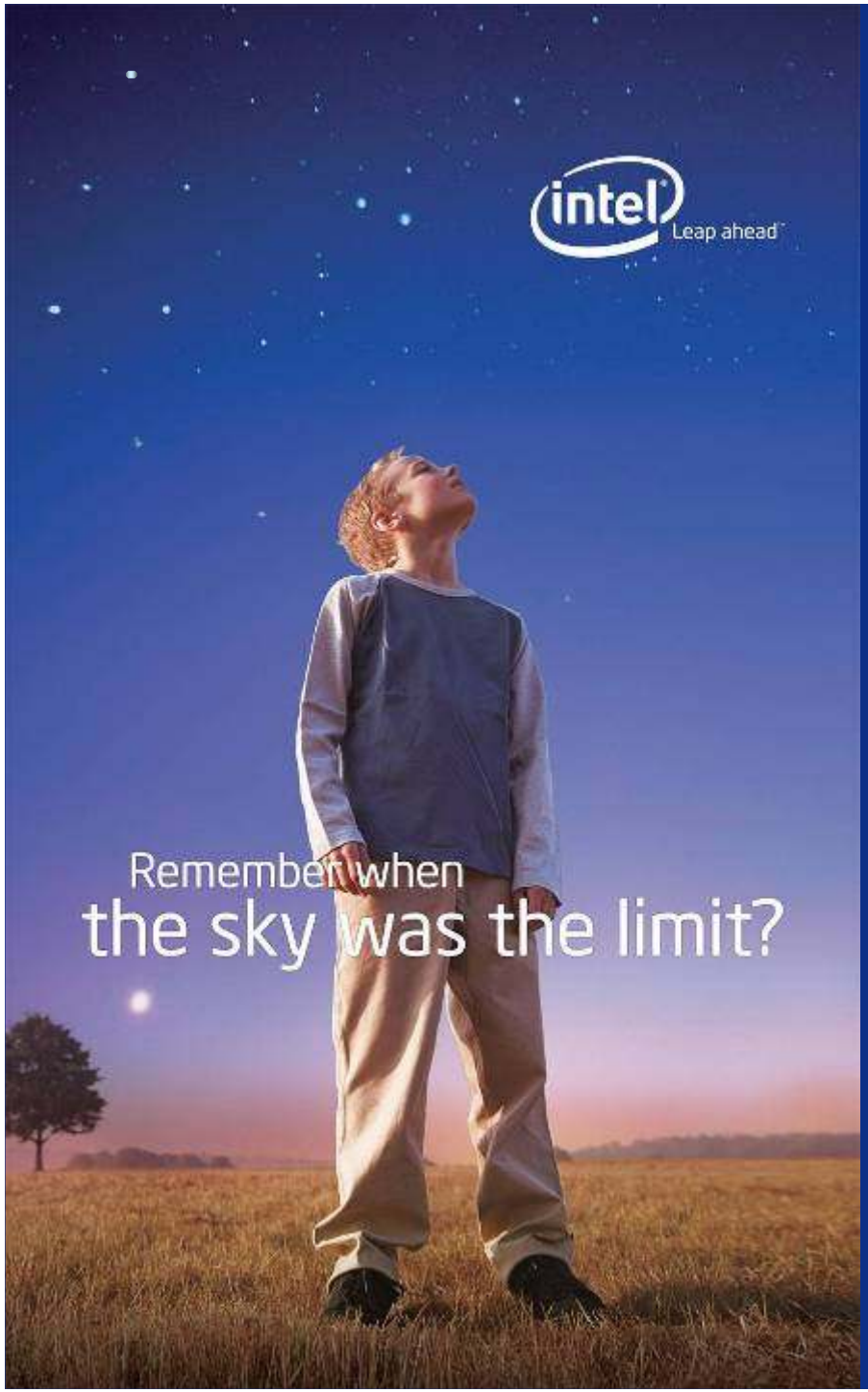
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Technology Impact On Your Products

Is this the story? What does this really mean?

- What are the top 10 semiconductor manufacturers driving towards?
 - Intel, Samsung, Texas, Toshiba, ST Microelectronics, Renesas Technology, Infineon Technologies, NEC Electronics, Hynix Semiconductor and AMD
- How does Moore's law really impact HPC?
- Silicon Technology is just size/area right?
- Direct Connect vs. FSB
- Cores:
 - When will we be at Multi-Cores?
 - Will there be Multi-Cores?

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Baseline

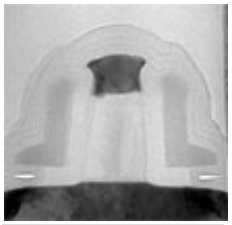
A General Perspective

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Silicon Future & Moore's Law what is the impact?

90nm 2003



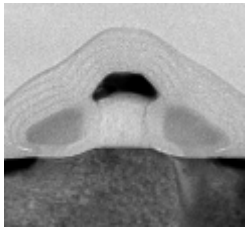
Initially Single Core

A Server 'way' meant 1 a core per socket

Beta on dual cores; Monectito and Dempsey

We Are Here

65nm 2005



Dual Core

A way now = 2cores

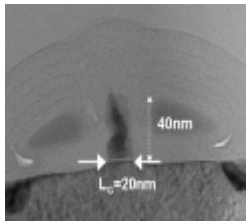
Each nm = 30% space

Beta Quad cores

A way = 4cores

Beta Direct Connect

45nm 2007



Quad Cores

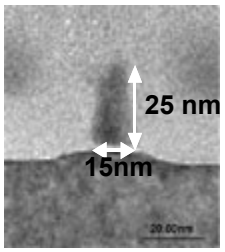
A way = 4cores

Gain 30% area never save power

Cores? Memory? Interconnect? Feature?

Beta Oct Cores?

32nm 2009



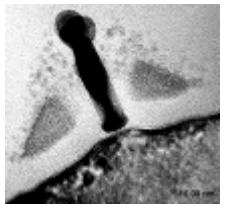
Oct Cores

Beta Multi-Cores

Direct Connect

???

22nm 2011



Integration drive: 2005 – 2012

Shouldn't we be saving Power?

Each Technology shift provides:

- **30% die space**
- **10% drop in volts gives 30% power saving cancelled by adding cores**

2013 – 2017

16nm 2013

11nm 2015

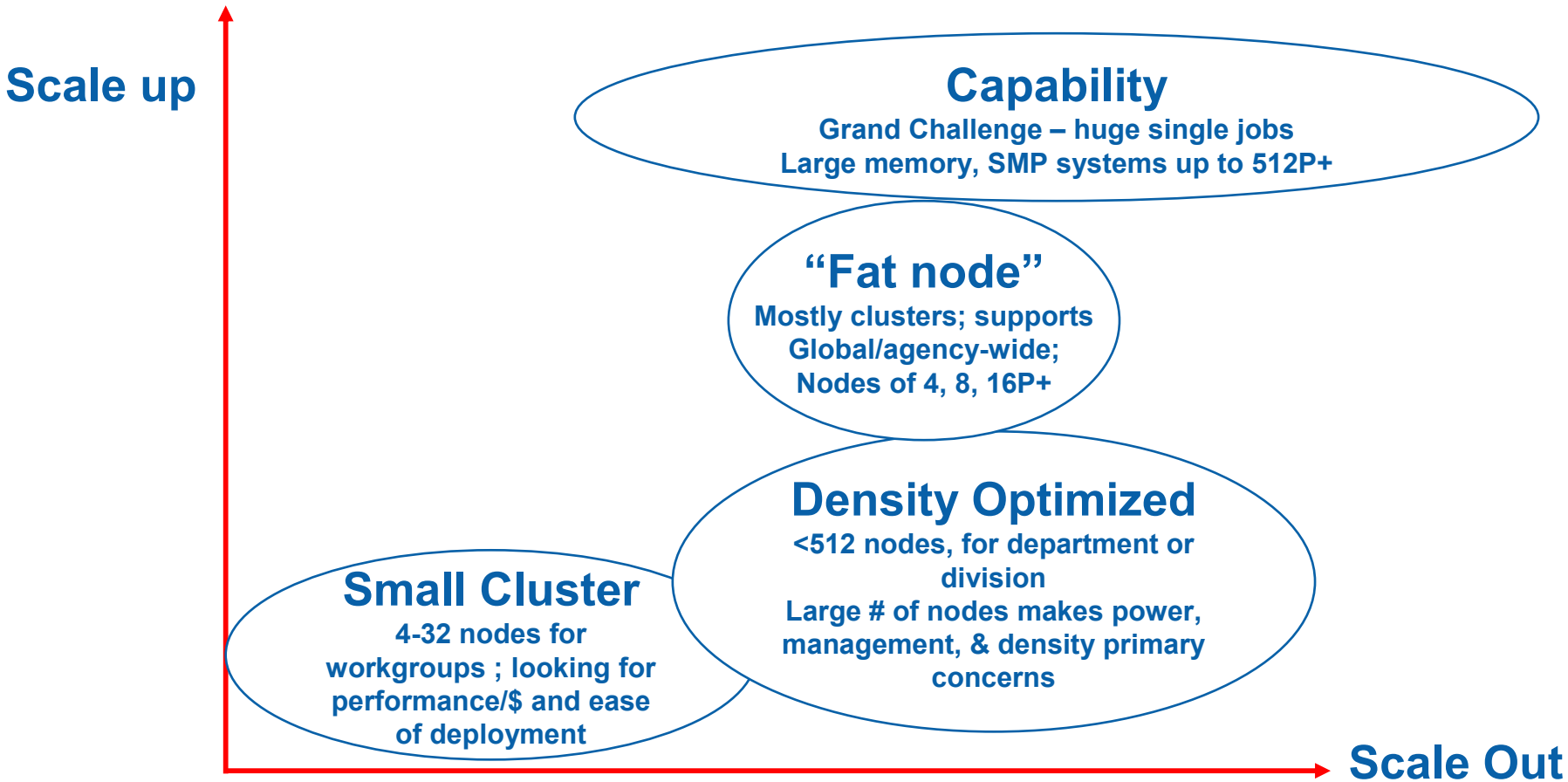
8nm 2017

Roadmap → **Research** →

New Intel technology generation every 2 years
Intel R&D technologies drive this pace well into the next decade

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Cores Raises Questions



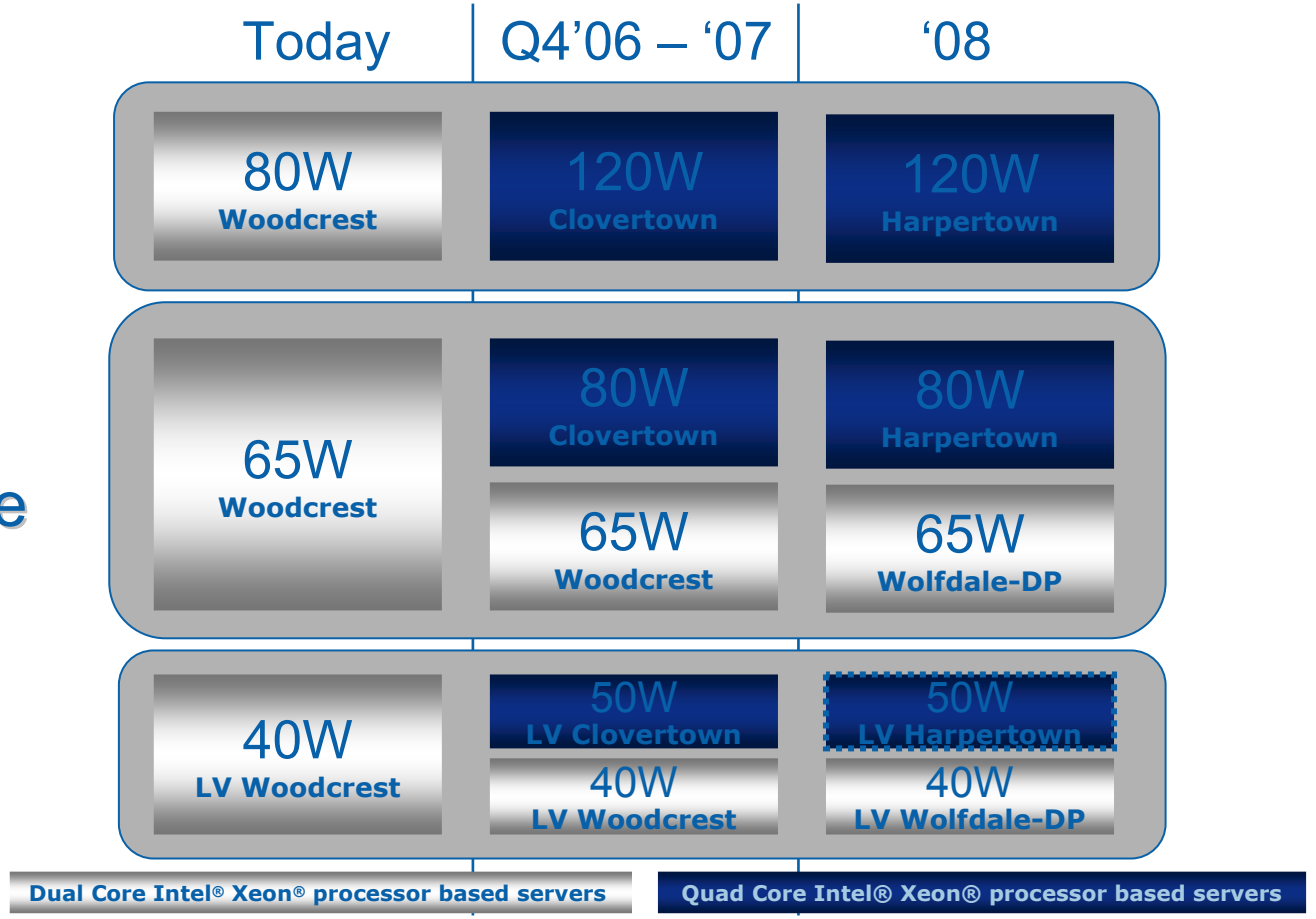
Small # of CPUs / nodes
>>> constantly shift

Large # of CPUs / nodes
Terror on a chip!

>> A Laptop Will Be A Fat Node (8 core) <<

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Intel® Xeon® DP Server & Workstation Platforms

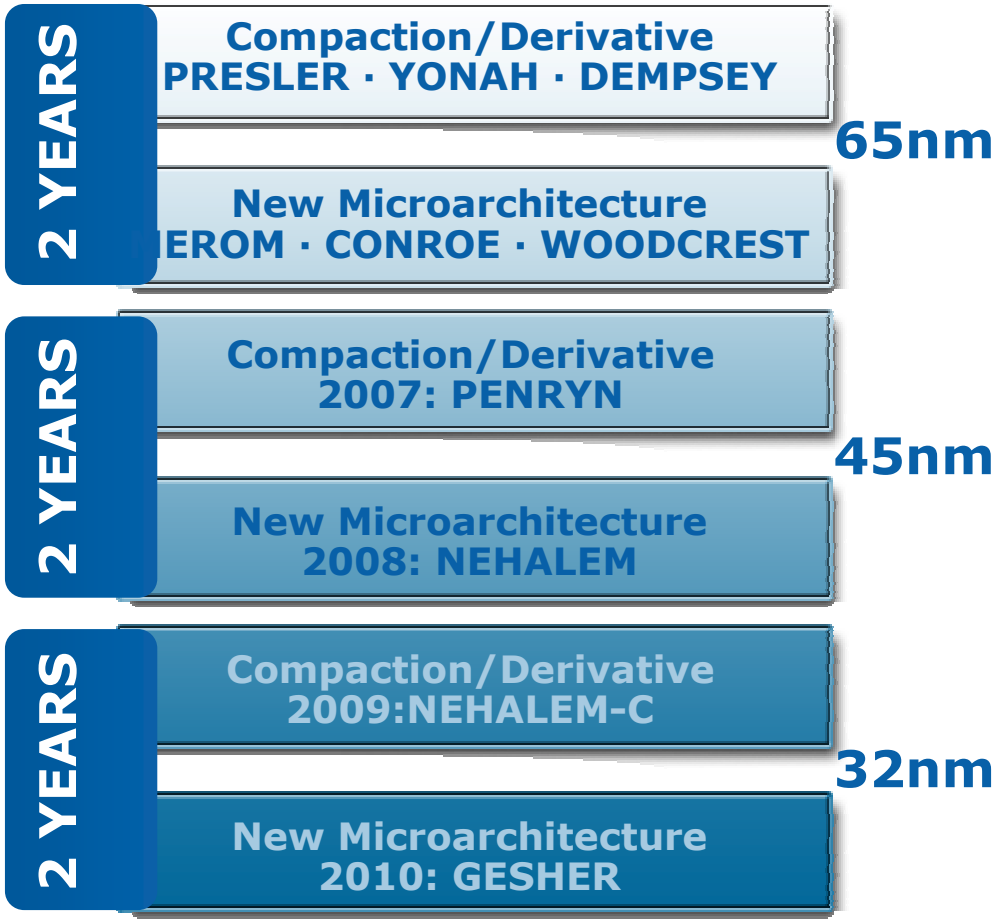


90%+ of processor volumes at ≤ 80W

Under consideration
Not POR

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Microprocessor Design Model Has To Evolve

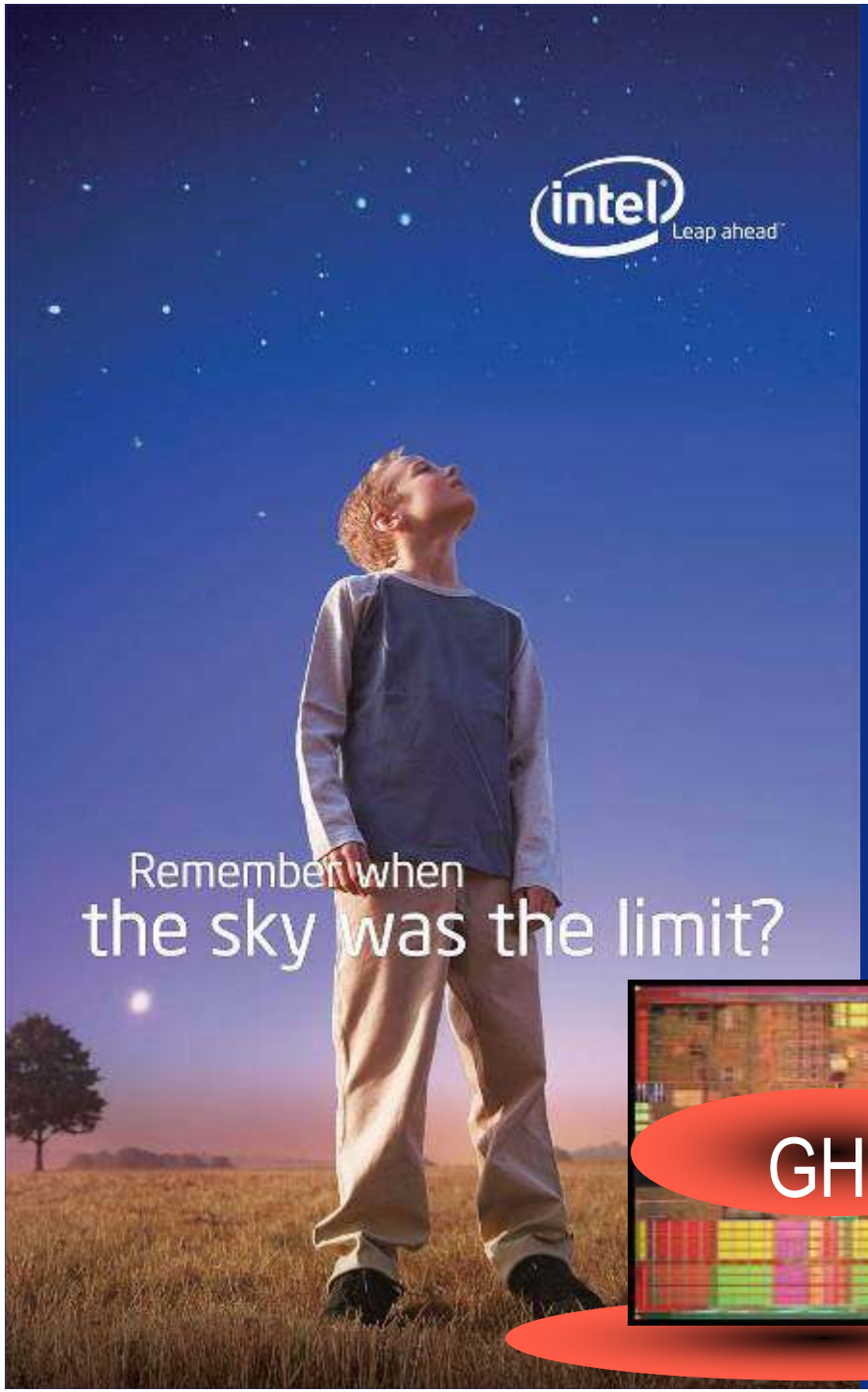


PRINCIPLES

1. One micro-architecture for all high volume market segments
2. Optimized for performance/watt
3. Parallel design teams
4. No waiting on new process technology
5. Chipset cadence offset for fast ramp

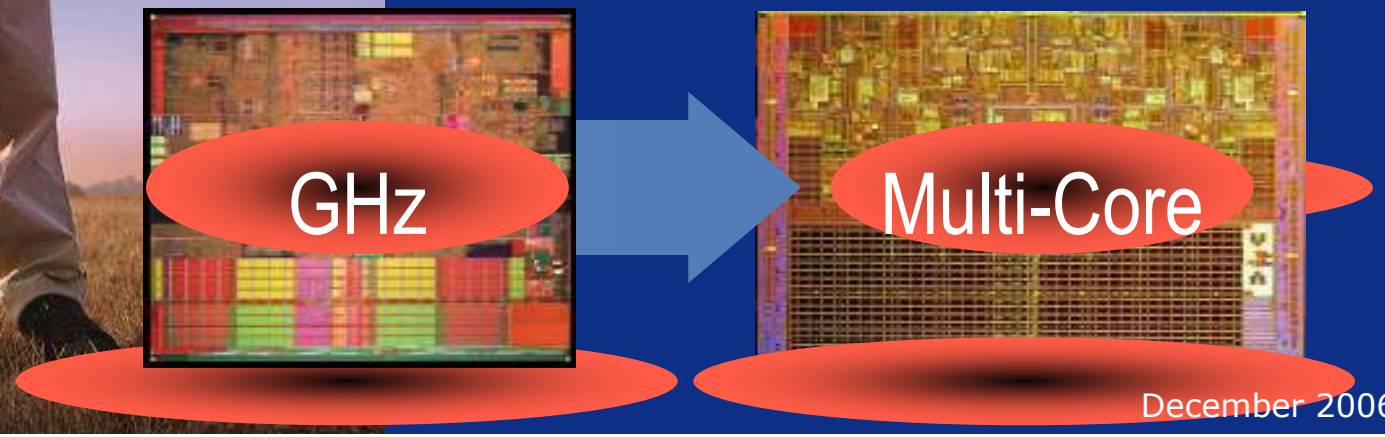
OBJECTIVE: Sustained Technology Leadership

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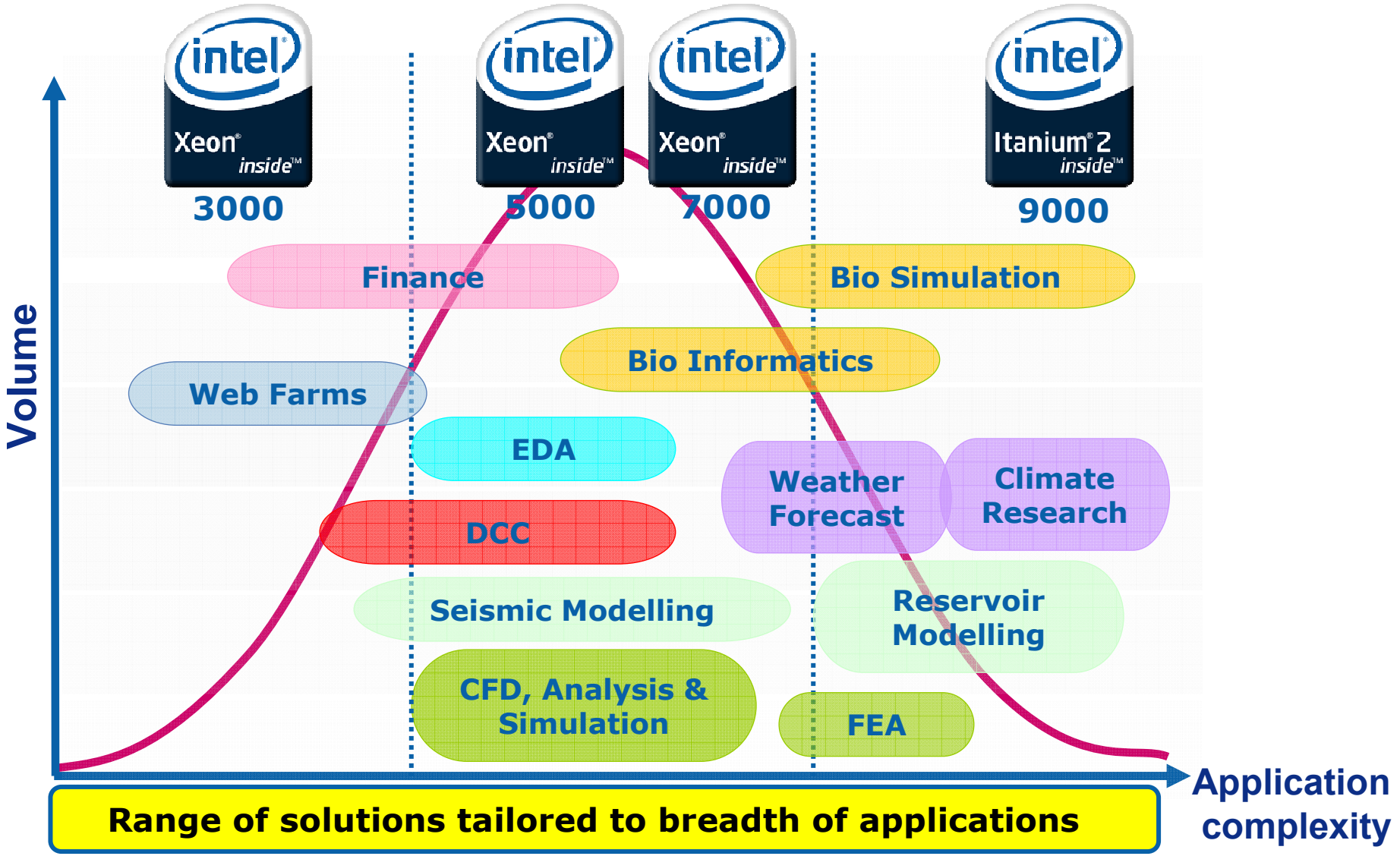
Come Clean

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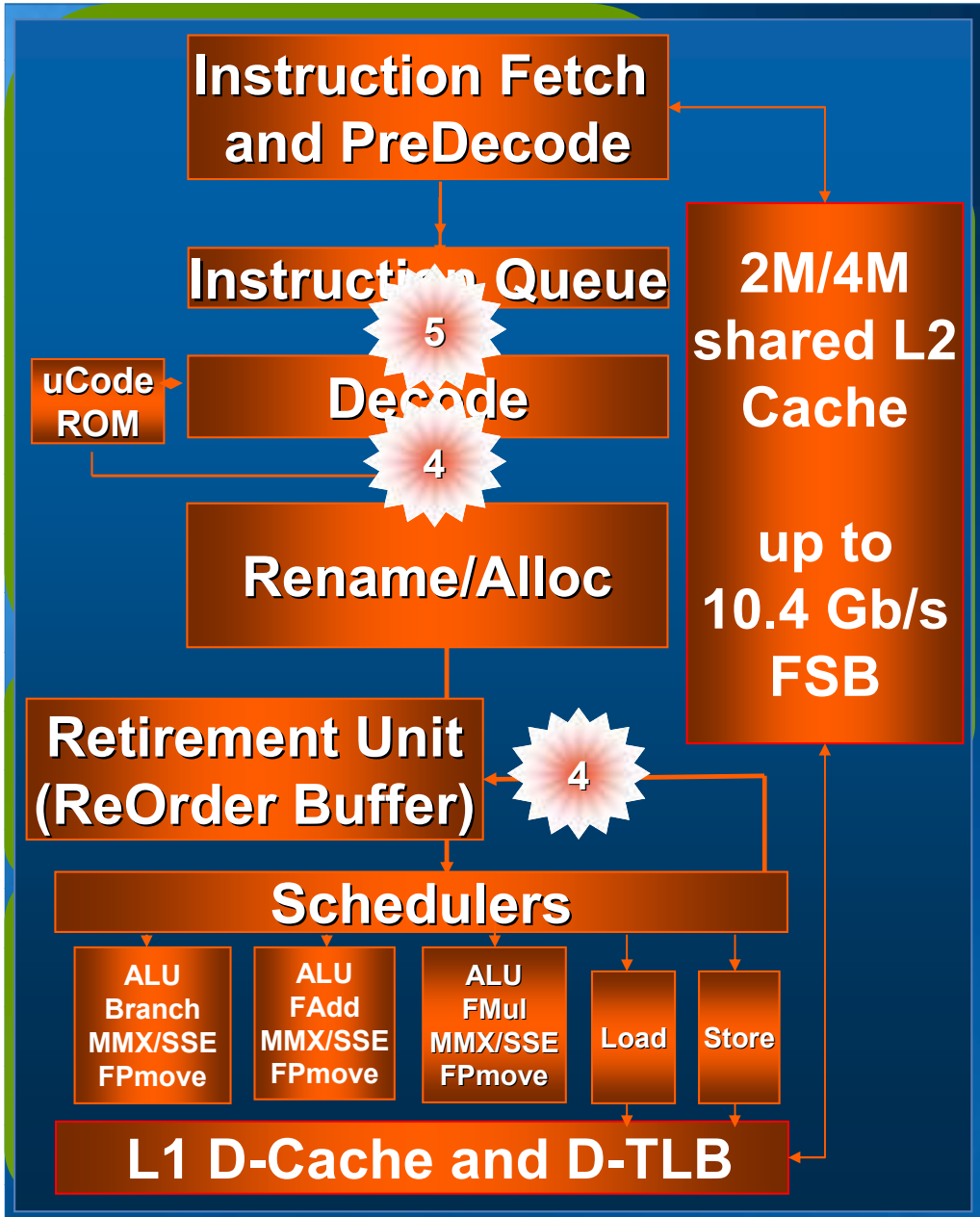
Hardware is the enabler –applications & efficiency is ?



This is not a complete guide to all applications/verticals

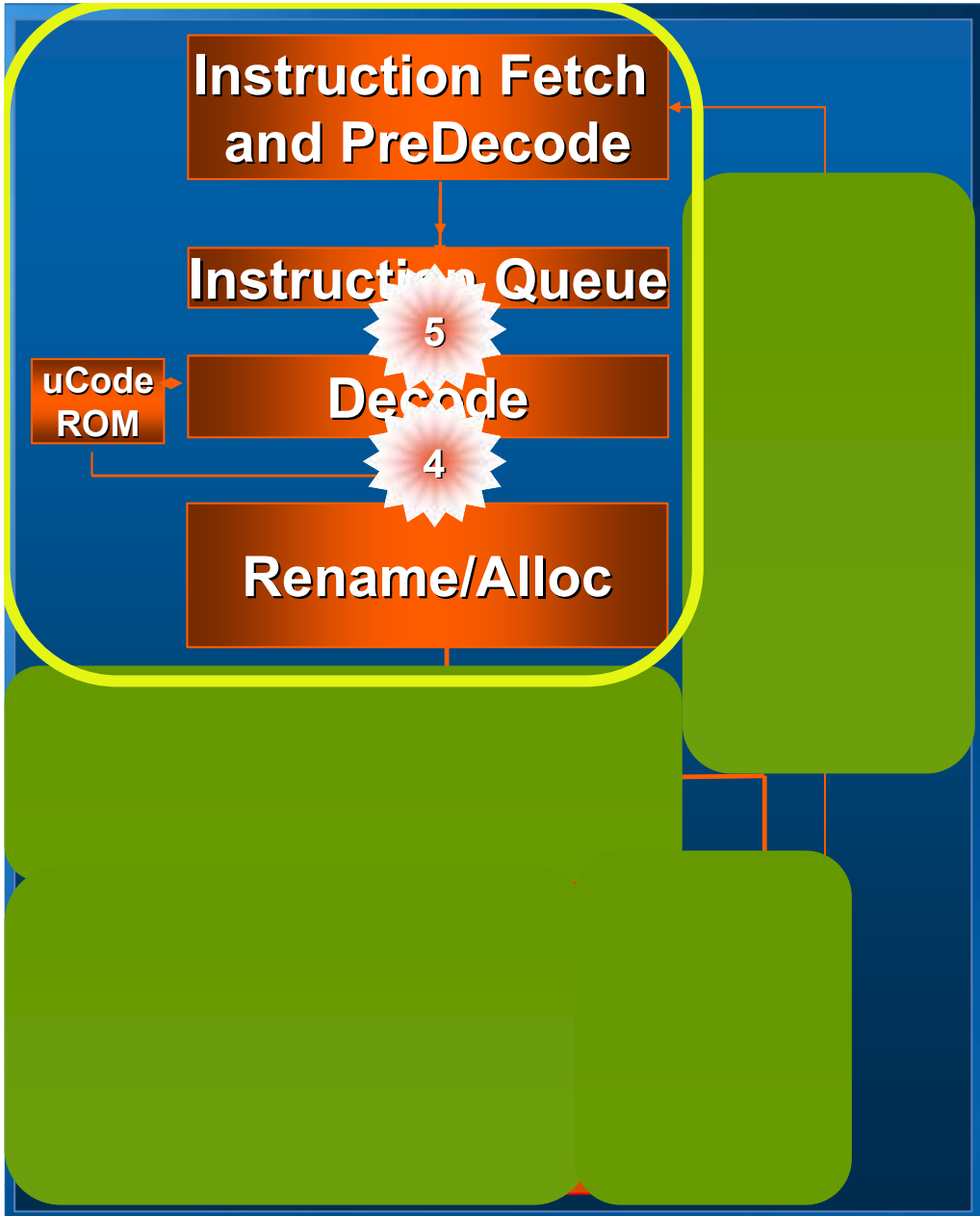
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Intel® Core™ Microarchitecture



A Core Walkthrough

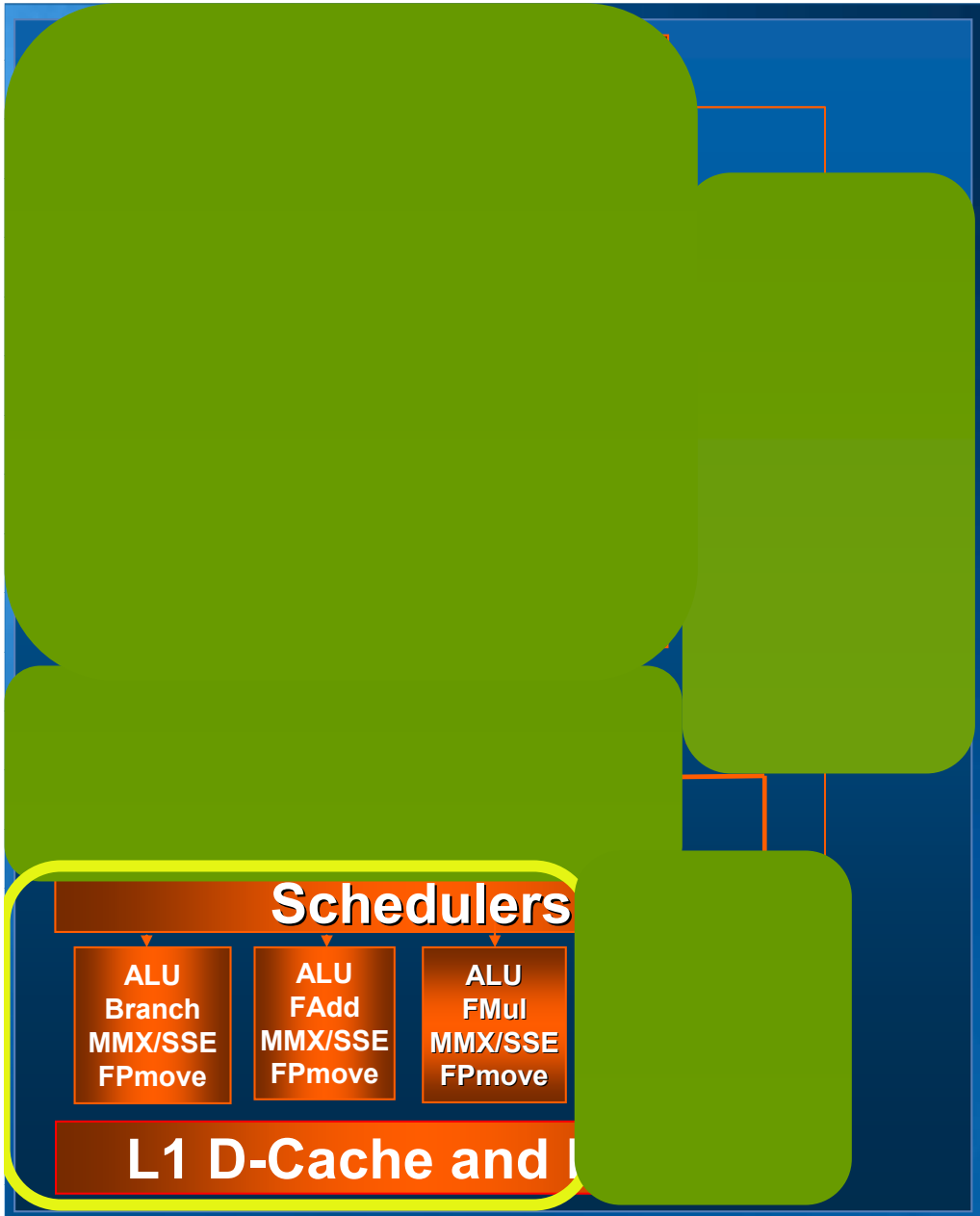
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in order

instruction fetch
instruction decode
micro-op rename
micro-op allocate

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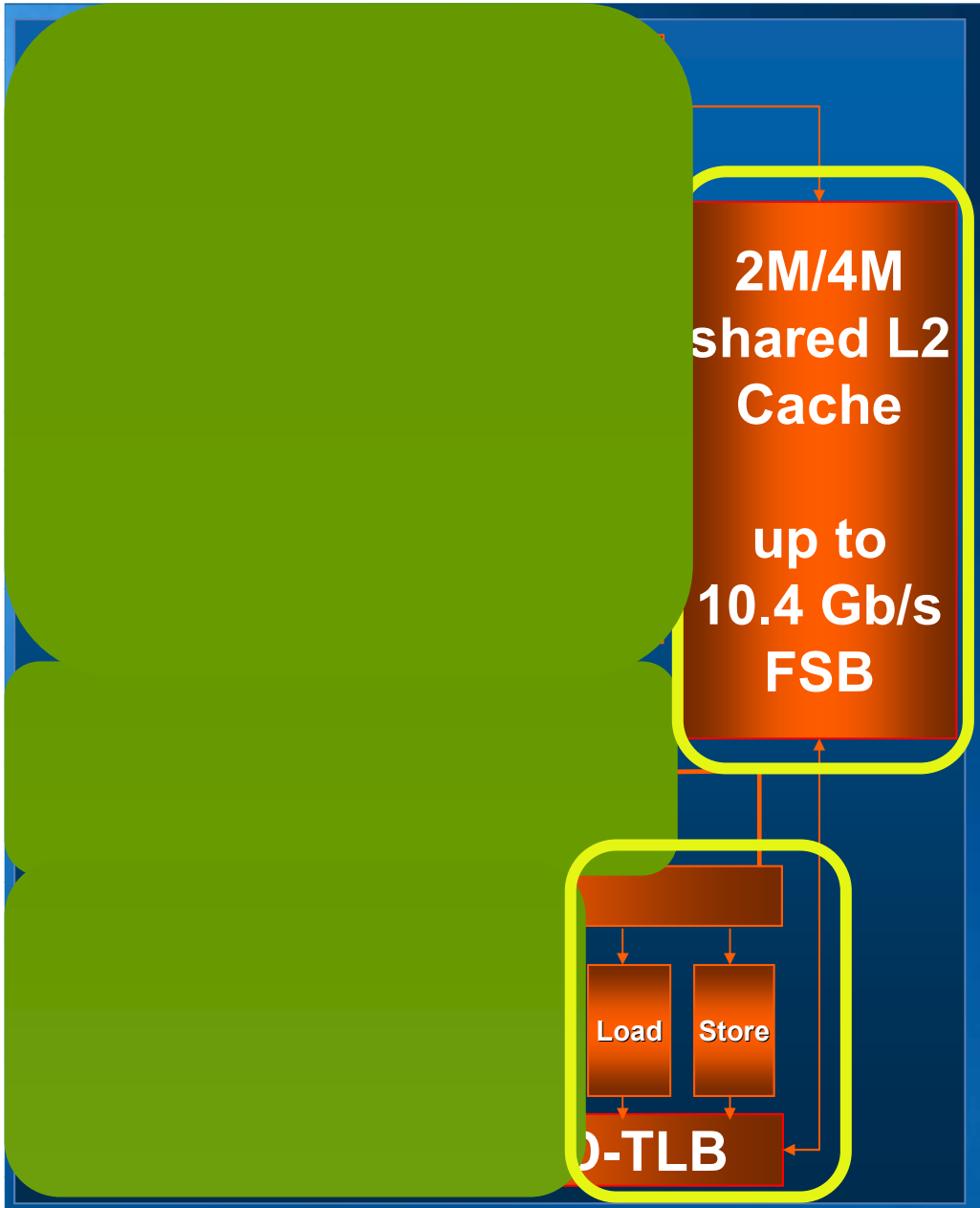


out of order

micro-op schedule
micro-op execute

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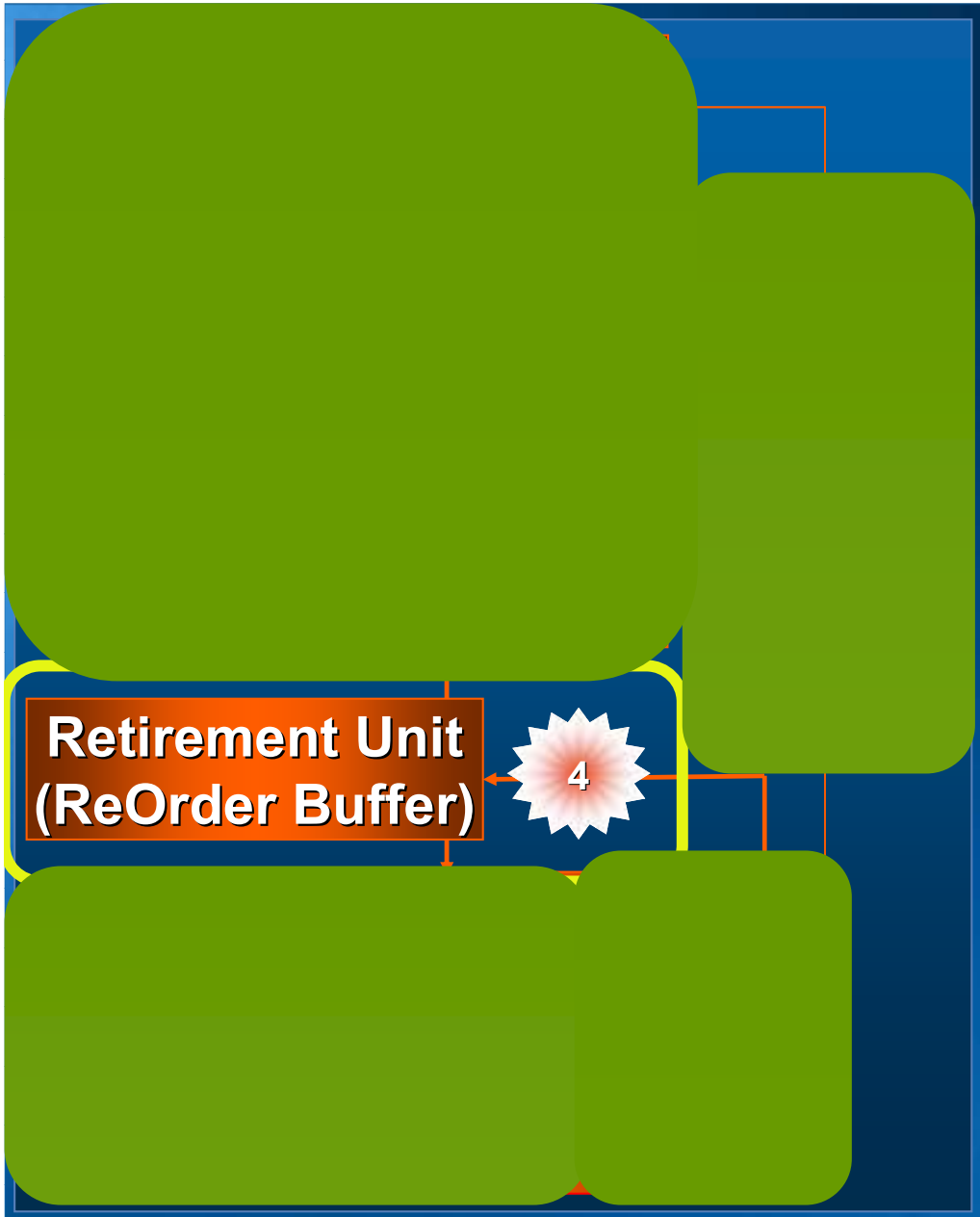
out of order

memory pipelines

memory order unit maintains architectural ordering requirements

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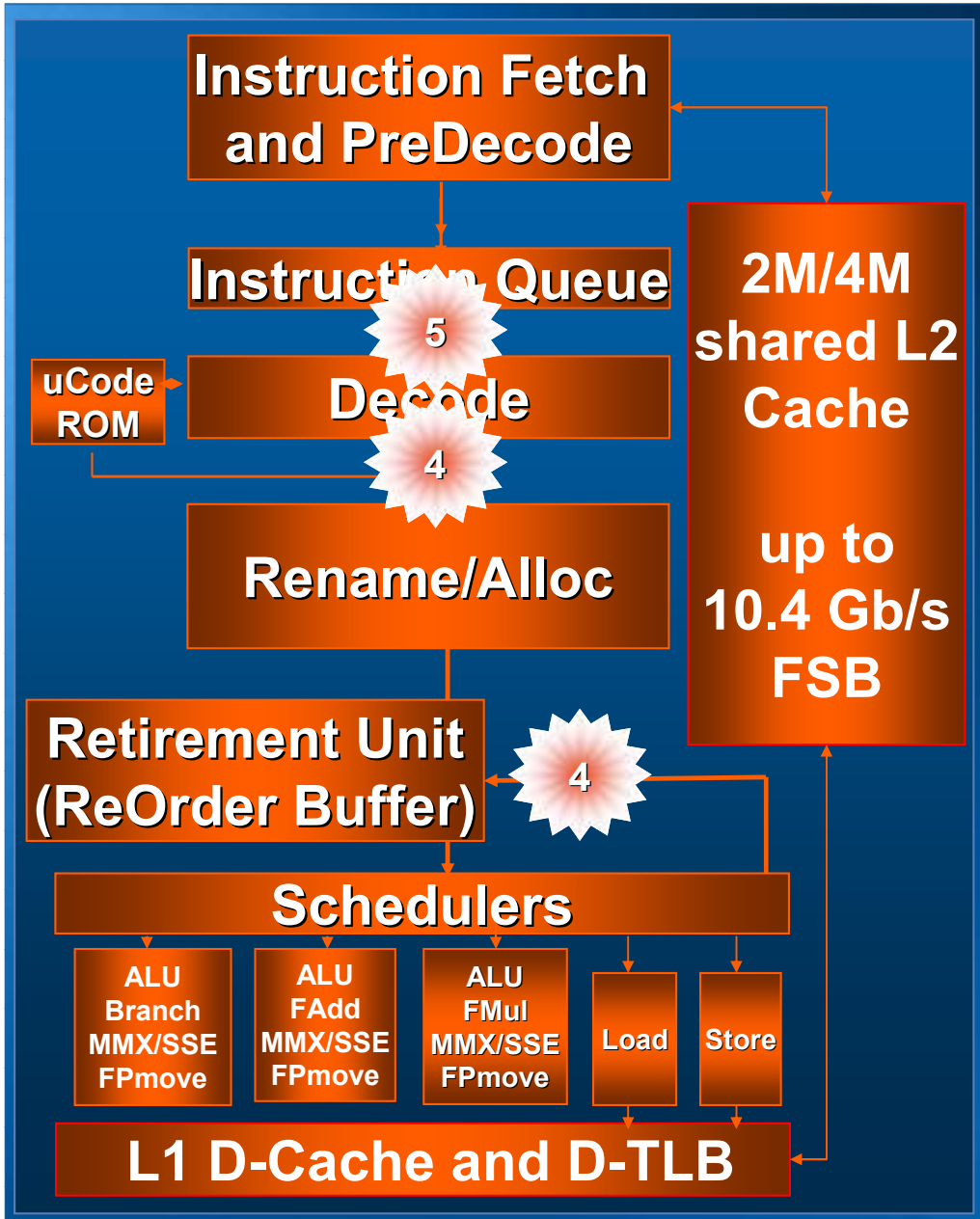
in order

micro-op retirement
fault handling

Retirement Unit maintains illusion of in order instruction retirement

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Intel® Core™ Microarchitecture
*n Cores Means….



- Step change in memory architectures
- Step change in Core definition
- Step change in Hardware efficiency
- Step change in Software efficiency/approach
- …Still Open Intel is in the race

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